Integrated Eight Element Ku Band Transmit/Receive Beamformer Chipset for Low-Cost Commercial Phased Array Antennas

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Abstract—An integrated eight element SiGe Ku band phased array and smart antenna beamformer chipset design is described. The beamformer chips include independent digital phase shifters and variable gain amplifiers in each of eight signal paths. The receive chip includes a low noise amplifier at each RF input, and the transmit chip includes a power amplifier at each RF output. Simulated performance meets design targets for the intended application to low-cost commercial phased array antennas for bidirectional satellite video and data ground terminals.

1. INTRODUCTION

Phased array antennas are moving beyond traditional applications in high-cost military radars and orbital platforms to low-cost terrestrial and commercial applications. The key cost driver for a phased array antenna is the beamformer electronics. For military and space-borne applications, beamforming is typically accomplished using a high-functionality T/R module which may include dozens of MMICs. Although T/R module costs have fallen significantly over the last decade, for commercial phased array applications, the cost per antenna element must be further reduced by an order of magnitude or more. To achieve this cost reduction, as much of the beamformer and signal handling electronics as possible must be integrated into a single ASIC that feeds multiple antenna elements.

Beamformer chips and chipsets are beginning to be developed in the research domain [1] as well as commercially for applications such as wireless routers and Wi-Max base stations. For some narrowband array applications such as ultrasound, integrated digital beamformers have been developed, but for commercial broadband, large-scale phased array application at RF and microwave frequencies, digital signal processing for every array element input/output channel is too costly. Consequently, most integrated beamformer development work relies on analog processing.

This paper reports on the development of an integrated Ku band SiGe BiCMOS transmit/receive beamformer chipset. The target applications for the beamformer chipset are smart antennas for fixed, mobile and in-motion direct broadcast satellite (DBS) receivers, very small aperture terminals (VSAT), and other broadband voice, data, and video satcom services. The receive beamformer chip operating bandwidth is 10-13 GHz, and the transmit beamformer chip bandwidth is 12-15 GHz, which accommodates all major worldwide Ku band uplink and downlink bands. Since the beamformer control relies on phase shifting rather than true time delay, the instantaneous bandwidth of the beamformer is limited by frequency-dependent beam squint, which in turn is determined by the largest dimension of the array aperture.

A major goal of this effort is to develop a beamformer chipset that has a real impact in enabling low-cost, commercial phased array antennas. This means that the development effort must result in more than a bench-top tested die. In order to realize a packageable, commercially viable component, the beamformer chip design must accommodate packaging parasitics, include ESD protection without degraded noise performance, be robust with respect to wide temperature variations, and have sufficient dynamic range to accommodate transmit-receive bleedthrough and radio frequency interference.

Both the receiver and transmitter chips are realized in 0.18-µm SiGe BiCMOS technology and measure 2.4 x 4.8 mm. In order to reduce the chip size and preserve a high directivity pattern of the combined signal, the phase shifting, amplification, and combining/splitting are performed in RF mode. Each chip incorporates a passive three-bit phase shifter that is based on a novel octagonal PIN diode SPST switch. An active topology for the splitter and combiner is used to ensure the proper channel-to-channel isolation and to compensate for the splitting insertion loss. Post-layout simulations used in the design of the presented transmit/receive beamformer took into consideration RLC parasitics of the layout interconnections as well as the packaging connectors.

2. FUNCTIONAL OVERVIEW

Functional diagrams for the receive and transmit beamformers are shown in Figures 1 and 2. The receive beamformer chip architecture includes low noise amplifiers (LNAs), digital phase shifters, variable gain amplifiers (VGAs), and an active power combiner. To maximize flexibility and enable dual-polarization beamforming, the eight element beamformer is divided into two independent, isolated four-element beamformers.

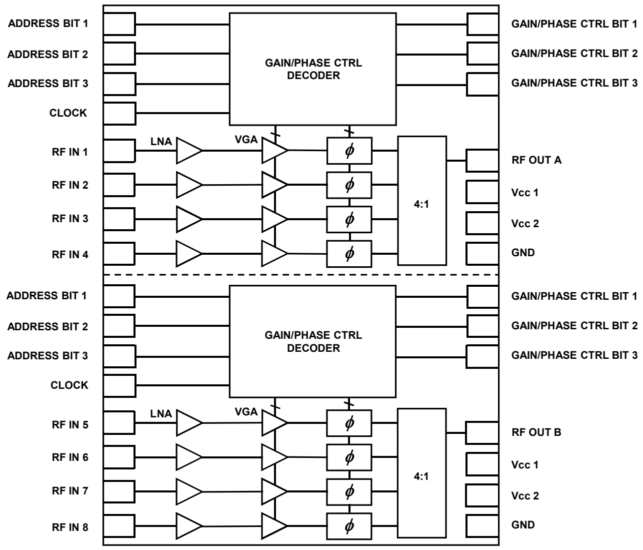

Figure 1. Receive beamformer functional diagram.

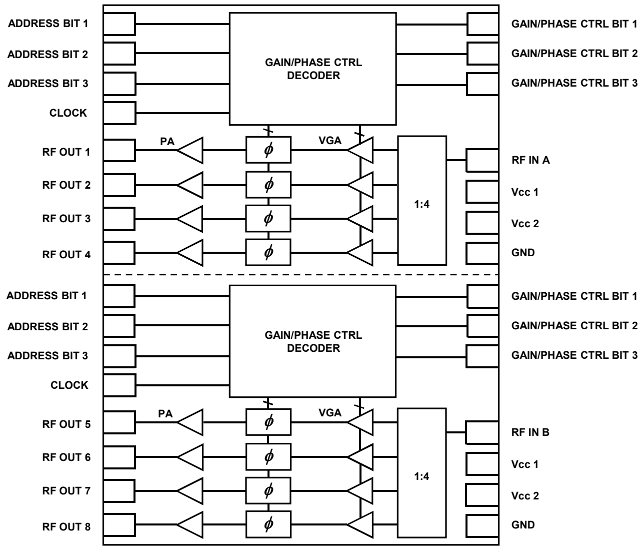

Figure 2. Transmit beamformer functional diagram.

Because the limiting factor in power-handling for the receive beamformer is the active combining network where signal levels are largest, this also provides increased dynamic range. For radar applications, high dynamic range is critical to avoid nonlinearity due to transmit signal bleedthrough into the receiver chains.

The designed noise figure for each receiver channel is 4 dB. For satcom applications that require lower noise figure, each antenna element is terminated with a discrete low-noise amplifier which feeds the beamformer chip RF inputs and provides enough gain that the equivalent receiver noise temperature is acceptably low. For applications with less stringent noise figure requirements, the elements can be directly connected to the beamformer chip RF inputs.

The transmit beamformer includes a power splitter, three-bit digital phase shifters, variable gain amplifiers, and power amplifiers. For large arrays with a low EIRP, the transmit beamformer chip can directly feed antenna elements. For small arrays or higher power applications, discrete power amplifiers are inserted between the transmit beamformer chip and antenna element input ports to provide additional gain and higher output power.

3. PHASE SHIFTER FOR RX AND TX BEAMFORMERS

The phase shifter is the most crucial component in phased array beamformers because the directional precision of a beam directly depends on the accuracy of the phase shift in each channel. Traditionally, phase shifters were implemented in GaAs IC technology or micro-electromechanical systems (MEMS) for high-end applications, but due to low integrative capabilities such implementations were very costly. Phase shifters can also be designed using MOSFET active circuitry; however, the off-state capacitance of a MOSFET would negatively impact the performance by limiting the bandwidth. The linearity would degrade as well because of the active nature of such design.

In order to increase the power handling capabilities of the phase shifter and reduce the power consumption, a passive phase shifter design will be used. The main principle behind the presented phase shifter design is steering the signal onto different paths that have a relative phase delay of 180°, 90° and 45°. Figure 3 depicts the topology of a 3-bit phase shifter [7]. The left-most bit provides the 180° shift and is based on a hybrid high-pass/low-pass topology. High-pass π-shape filter provides the least negative phase delay thus serving as a reference path while the low-pass T-shape filter serves as the delay path. The 90° and 45° bits (center and right, respectively) use a bridged-T type filter. When the MOSFET switches M1 and M2 are turned on, they form a low-pass T-type filter that provides a phase delay relative to the reference upper path. When these switches are turned off, their off-state capacitances would form the LC-tank with shunt inductors L5 and L7. D1 and D2 PIN diodes are used as single-pole single-throw (SPST) RF switches enabling or disabling the reference path while D3 and D4 PIN diodes are used to enable/disable the phase delay path. Similarly, D5 and D6 PIN diodes are used to enable/disable the reference paths for the 90° and 45° bits, respectively. C1, C4, C5, C6, C8, C9 and C11 are DC blocking capacitors. Each PIN diode consumes about 1 mA in forward-biased mode, so the maximum current of 4 mA will occur during the reference phase (0°) and the minimum current of 2 mA will occur during the 135° and 315° phase shifts.

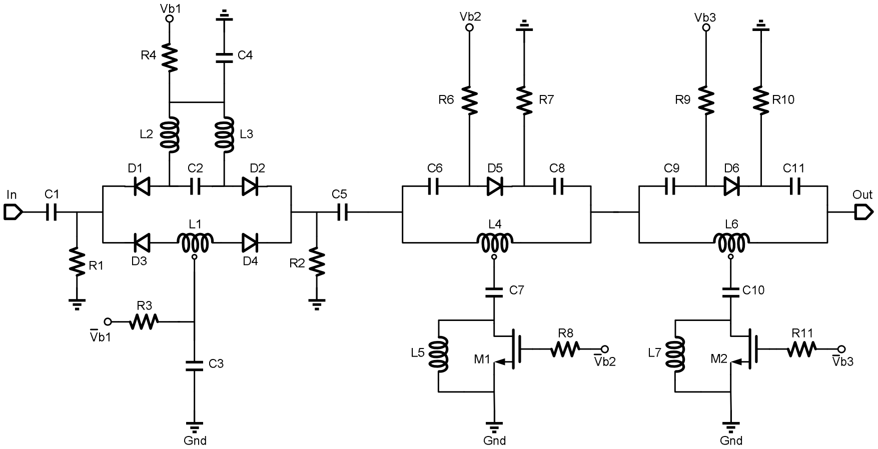

Figure 3. Schematic of the proposed 3-bit phase shifter

A novel octagonal PIN diode is one of the crucial elements in the phase shifter design. Its performance as the SPST switch will greatly influence the overall performance of the phase shifter. Conventional PIN diodes mostly have been implemented in GaAs or InP technologies which prevented them from being integrated into low-cost SiGe process. The PIN diode used in this paper was custom designed in a standard 0.18-µm SiGe BiCMOS technology by using HBT layers: P+ base layer, N-epi collector layer and buried N+ subcollector layer [11]. The vertical cross-sectional view of this PIN diode is shown in Figure 4.

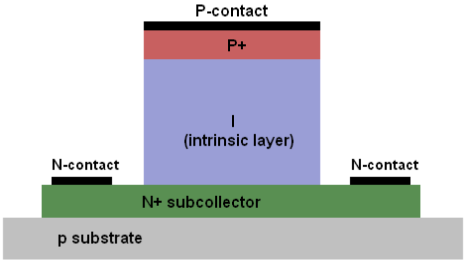

Figure 4. Vertical PIN diode cross-sectional view

For the PIN RF switch, the crucial performance criteria are the forward bias insertion loss and the reverse bias isolation. This novel octagonal PIN diode provides the return loss of better than 24 dB, isolation of 27 dB to 10 dB over the 2 – 18 GHz frequency range and an insertion loss of just under 0.7 dB [8].

4. Low Noise Amplifier (LNA) for RX Beamformer

Low noise amplifiers (LNAs) are one of the most challenging components in beamformer receivers. LNAs need to be impedance matched to the antenna over the entire operating frequency range of the beamformers. To meet the receiver sensitivity requirement, LNAs also need to achieve high gain and low noise figure [1, 2]. In this design, we are aiming at a high gain of 15 dB to minimize the noise contribution of the following stages to the receiver system.

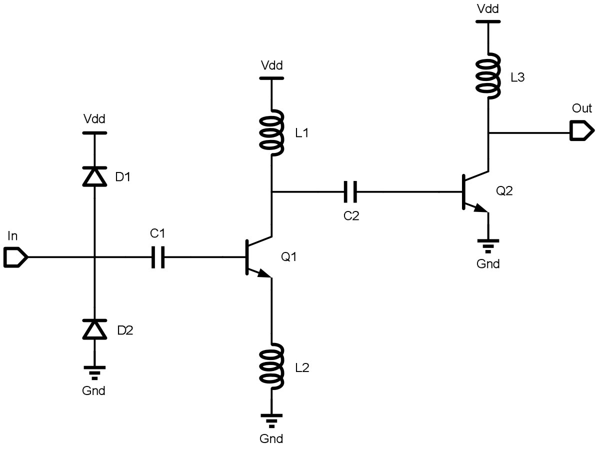

Figure 5. Schematic of the proposed LNA

The schematic of the proposed LNA is shown in Figure 5 which consists of two common emitter amplifiers. C1 and C2 are DC blocking capacitors. L1 and L3 are RF choke inductors as well as loads of the first and second stage amplifiers, respectively. L2 is an emitter degeneration inductor. As the LNA is the first stage in the receiver, ESD (ElectroStatic Discharge) diodes are included at the input of the first stage.

5. VARIABLE GAIN AMPLIFIER (VGA) FOR RX AND TX BEAMFORMERS

Variable gain amplifiers (VGAs) have been widely used in many applications like wireless communication receivers, and beamformers. In general, the design of VGAs needs to meet requirements in gain, bandwidth, noise, linearity under power consumption and die area constraints [3, 4]. The VGAs in beamformers are able to increase the dynamic range of the overall beamformer systems as well as to set different power levels for various phases. Generally, there are two approaches used to realize VGAs depending on whether the control signal is digital or analog. In this proposed VGA, digital control signal is used with current steering mechanism for different gains. In our design, the VGA in the receiver has exactly the same architecture as that in the transmitter, but the operating frequency ranges are different, so the circuit parameters are optimized for the receive and transmit bands, respectively.

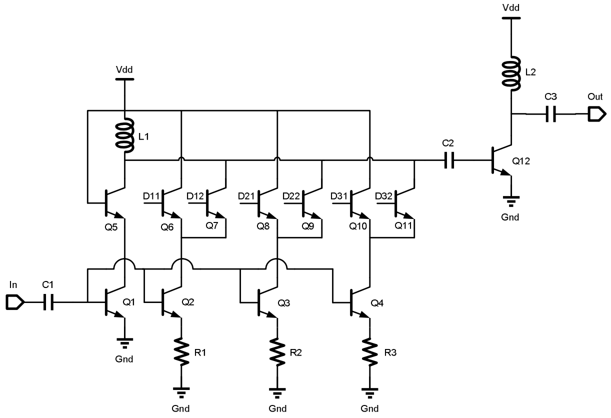

Figure 6. Schematic of the proposed VGA

The schematic of the proposed VGA is shown in Figure 6. C1, C2 and C3 are DC blocking capacitors. L1 and L2 are RF choke inductors as well as loads of the first and second stage amplifiers, respectively. R1, R2 and R3 are emitter degeneration resistors. Q1 and Q5 form a fixed gain path, providing the minimum gain of this VGA. Q2, Q3 and Q4 have different current weightings and Q6-Q11 are switches determining the current flow directions of collector currents of Q2, Q3 and Q4. When D11, D21 and D31 are high, these collector currents are bypassed and when D12, D22 and D32 are high, these currents are flowing into the base of the second stage BJT and will be amplified. To improve the linearity of the VGA, a diode linearizer is designed.

6. POWER AMPLIFIER FOR TX BEAMFORMER

Power amplifiers (PAs) account for a significant portion of energy consumption in beamformer transmitters. Improving the power efficiency of PAs is especially important for mobile applications because the battery life is limited. Meanwhile, there are stringent linearity constraints on PAs in beamformer systems employing non-constant envelope signals. It remains a challenge in PA design to achieve high efficiency while maintaining low distortion [5, 6]. In this design, our main targets are output P1dB of 12 dBm, gain of 15 dB and power efficiency of more than 25%.

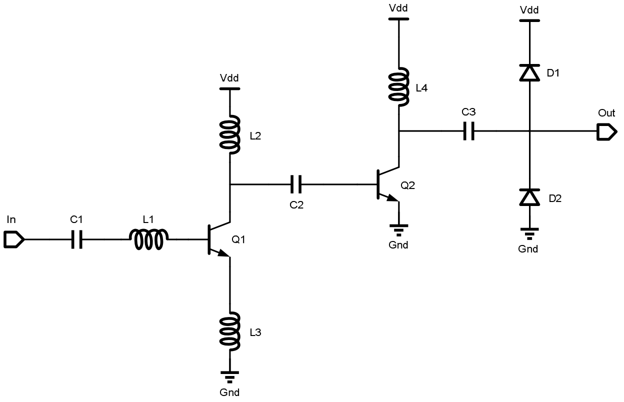

Figure 7. Schematic of the proposed PA

Figure 7 is the schematic of the proposed PA, which is composed of two cascaded common emitter amplifiers. C1, L1 and emitter degeneration inductor, and L3 works as input matching network. L2 and L4 are RF choke inductors as well as loads of the first and second stage amplifiers, respectively. An adaptive bias circuit is designed to improve the linearity of the PA. As the PA is the last stage in the transmitter, ESD (ElectroStatic Discharge) diodes are included at the output of the second stage.

7. POWER SPLITTER FOR TX BEAMFORMER

A power splitter is used in the transmit beamformer to split the incoming RF signal into four identical signals; therefore it is very important to ensure that the split signals have the same phase and the same magnitude. In order to improve the channel-to-channel as well as inverse isolation, an active topology was implemented. To satisfy the overall TX output-referred P1dB of 12 dBm, the power splitter should have an output-referred P1dB of at least -5 dBm. The active topology of the splitter can also provide some gain to compensate for the loss due to passive phase shifter.

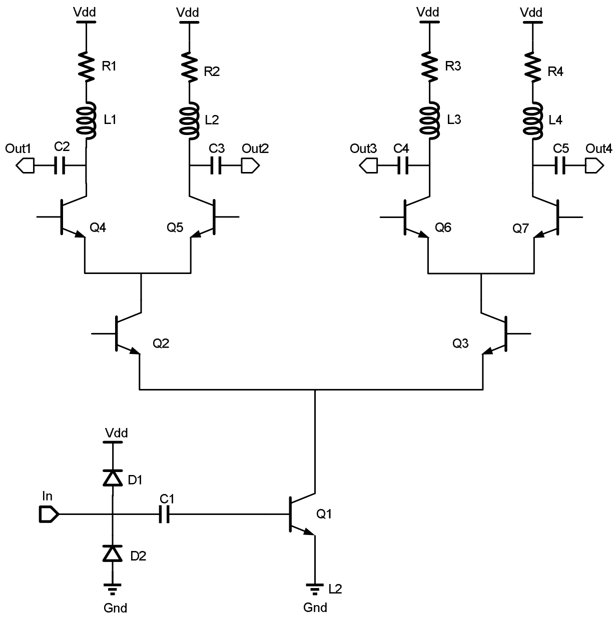

Figure 8. Schematic of the proposed power splitter

Figure 8 depicts the schematic of the proposed power splitter which consists of four cascode amplifier branches. Resistors R1-4 and inductors L1-4 are used as the loads, and C1-5 are DC blocking capacitors. A resistive component is added to the load in order to improve broadband performance. A diode linearizer is designed to improve the linearity of the power splitter. Because the power splitter is the first stage of the transmitter, ESD diodes D1 and D2 are added at the input.

8. Power Combiner for RX Beamformer

A power combiner is used in receive beamformer to combine four RF signals into one outcoming signal; therefore it is important to ensure that while signals are being combined, their phase and magnitude do not change due to the possibility of asymmetrical branches. In order to improve the channel-to-channel as well as inverse isolation, an active power combiner topology was implemented. In addition, the active combiner can compensate for the loss due to passive phase shifter.

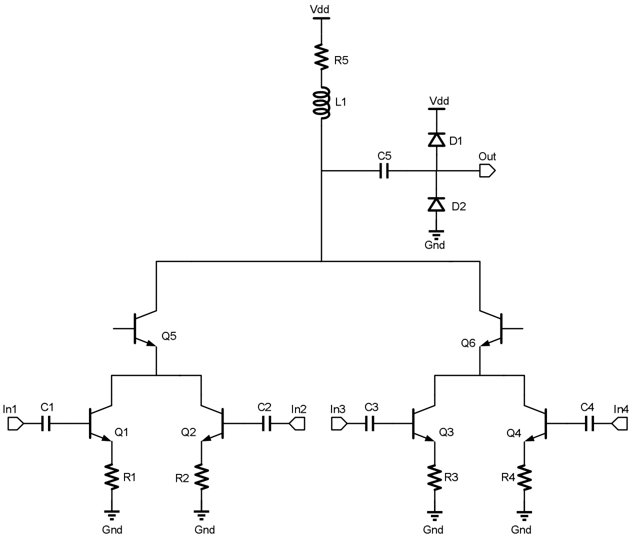

Figure 9. Schematic of the proposed power combiner

Figure 9 depicts the schematic of the proposed power combiner which consists of four symmetrical input stages. The signal is then combined through the cascode BJTs. R1-4 are served as the degeneration resistors used to improve input matching, and inductor L1 along with resistor R5 are used as the load to provide for better broadband performance. C1-5 are DC blocking capacitors. Because the power combiner is the last stage of the receiver, ESD diodes D1 and D2 are added at the output.

9. TX and RX Beamformer Performance

The simulated performance of the RX and TX beamformers including all package parasitics and layout parasitics are presented in tables 1 and 2, respectively.

Table 1. Simulated performance of the receiver

Supply Voltages	1.8 V, 3.3 V
DC Power Consumption	822 mW
RF Input/Output Frequency	10 - 13 GHz
RF Input/Output Impedance	50 Ω

Gain (One RF IN To RF OUT) At Maximum VGA Setting	15.46dB@11.5GHz
VGA Gain Range	-0.5 dB to 13 dB
Gain Settling Time	< 1 us
Gain Stability Over Temperature	0.023dB/°C@11.5GHz
Gain Flatness Over Any 50 MHz Bandwidth	0.1 dB
Gain Stability Over Phase States	±2.2 dB
Phase Range	360°
Phase Settling Time	< 1 us
Phase Stability Over Temperature	0.5°/ °C@11.5GHz
VGA Phase Stability	0.15°/dB@11.5GHz
Maximum Phase Length Difference Over All Eight RF Signal Paths	< 2°
Group Delay Flatness Over Any 50 MHz bandwidth	0.9 ps
RF Input VSWR	1.21:1@11.5GHz
RF Output VSWR	1.03:1@11.5GHz
Noise Figure	4.8dB@11.5GHz
Intermodulation Distortion	-53dBc
P1dB at LNA Output	6.6dBm @11.5 GHz

Table 2. Simulated performance of the transmitter

Supply Voltages	3.3 V/1.8 V
Supply Current	186 mA/364 mA
DC Supply Power At Maximum RF Output Power (30 mW/Channel)	1.27 W
Power Added Efficiency (PA Only)	17.4%
RF Input/Output Frequency	12.5 – 14.7 GHz
RF Input/Output Impedance	50 Ω
Gain (One RF IN To RF OUT) At Maximum VGA Setting	23.8 dB @ 13.6 GHz
VGA Gain Range	12.84 dB @ 13.6 GHz
Gain Settling Time	<1 µs
Gain Stability Over Temperature	0.11 dB/°C @ 13.6GHz
Gain Stability over Phase States	±1.3 dB (max)
Gain Flatness Over Any 50 MHz Bandwidth	0.16 dB
Phase Range	360°
Phase Settling Time	<1 µs
Phase Stability Over Temperature	0.36°/ °C @ 13.6 GHz
VGA Phase Stability	0.50°/dB @ 13.6GHz
Maximum Phase Length Difference Over All Eight RF Signal Paths	1.5°
Group Delay Flatness Over Any 50 MHz bandwidth	3.2 ps
RF Input VSWR	1.15:1 @ 13.6 GHz
RF Output VSWR	1.30:1 @ 13.6 GHz
Intermodulation Distortion	-58 dBc
Output P1dB	12.09 dBm @ 13.6 GHz

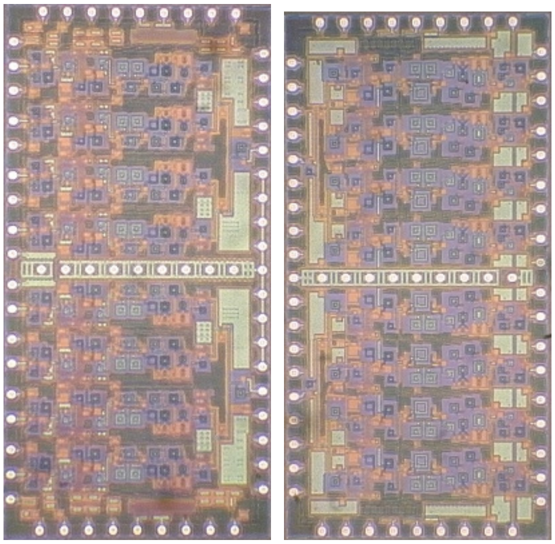

Figure 10. Microphotograph of (left) RX (2.4 mm x 4.8 mm) and (right) TX (2.4 mm x 4.8 mm) fabricated beamformer chips.

10. TRANSMITTER AND RECEIVER CHIP LAYOUTS

Microphotographs of the fabricated RX and TX chips are presented in Figure 10. Each chip including pads measures 2.4 x 4.8 mm. The layout of the pads and their arrangement was aimed at making them compatible with flip-chip packaging. The increased number of ground pads in the middle of the chip provide for reduced RF ground parasitics.

11. CONCLUSIONS

The beamformer chip design described in this paper has been fabricated and die are currently in testing. Test structures show that the basic functional blocks are operative, and the Tx and Rx beamformer chips are undergoing packaging and detailed characterization. We anticipate that the Ku band beamformer chipset will enable a significant reduction in the cost of phased array antennas for commercial satellite voice, data, and video communications terminals.

ACKNOWLEDGEMENTS

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